PATENT NUMBER and ISSUE DATE

U.S. **UTILITY** Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10081652	02/21/2002	~~710~~ 711	100	~~2181~~ 2184	~~Lhuong~~ Ray

**APPLICANTS: LaBerge Paul;

**CONTINUING DATA VERIFIED:

** FOREIGN APPLICATIONS VERIFIED:

PG-PUB	DO NOT PUBLISH ☐	RESCIND ☐

Foreign priority claimed	☐ yes ☐ no	ATTORNEY DOCKET NO
35 USC 119 conditions met	☐ yes ☐ no	501128.01
Verified and Acknowledged Examiners's intials		

TITLE : Memory bus polarity indicator system and method for reducing the affects of simultaneous switching outputs (SSO) on memory bus timing

U.S.DEPT. OF COMM./PAT.& TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		Assistant Examiner	CLAIMS ALLOWED	
			Total Claims	Print Claim for O.G
ISSUE FEE			DRAWING		
Amount Due	Date Paid		Sheets Drwg.	Figs.Drwg.	Print Fig.
		Primary Examiner			
☐ TERMINAL DISCLAMER		PREPARED FOR ISSUE	Application Examiner		

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